WHAT IS CLAIMED IS:

1. A system for compensating for phase differences between a plurality of signals associated with a plurality of signal levels, comprising:

at least one phase comparator for comparing a phase of a first signal associated with a first signal level with a phase of a second signal associated with a second signal level, and for generating at least one compensation signal indicative of a phase difference between the first signal and the second signal; and

at least one delay adjuster coupled to the at least one phase comparator and responsive to the at least one compensation signal, for delaying the first signal to compensate for the phase difference between the first signal and the second signal.

2. The system of claim 1 wherein the at least one delay adjuster comprises at least one adjustable delay buffer.

3. The system of claim 2 wherein the at least one phase comparator comprises:

a rising edge phase comparator for comparing a rising edge of the first signal with a rising edge of the second signal, for generating at least one rising edge compensation signal indicative of a phase difference between the rising edge of the first signal and the rising edge of the second signal; and

a falling edge phase comparator for comparing a falling edge of the first signal with a falling edge of the second signal, for generating at least one falling edge compensation signal indicative of a phase difference

between the falling edge of the first signal and the falling edge of the second signal.

4. The system of claim 1 wherein the at least one adjustable delay buffer:

delays the rising edge of the first signal in response to the rising edge compensation signal; and

delays the falling edge of the first signal in response to the falling edge compensation signal.

5. The system of claim 2 wherein the at least one adjustable delay buffer comprises:

at least one buffer transistor for buffering the first signal; and

at least one control transistor, responsive to the at least one compensation signal, for adjusting current flow through the at least one buffer transistor for controlling delay of the first signal through the at least one buffer transistor.

6. The system of claim 1 further comprising a plurality of buffers for generating the first signal and the second signal.

7. The system of claim 6 wherein the plurality of buffers comprise a plurality of clock trees.

8. The system of claim 1 further comprising at least one power supply for providing a plurality of supply voltages associated with the plurality of signal levels.

9. The system of claim 1 wherein the first signal and the second signal are derived from a common clock signal.

10. A system for compensating for phase differences between a plurality of signals, comprising:

a level adjuster for modifying a signal level of a signal to generate a first signal associated with a first signal level that is different than a second signal level associated with a second signal;

at least one phase comparator for comparing a phase of the first signal with a phase of the second signal, and for generating at least one compensation signal indicative of a phase difference between the first signal and the second signal ; and

at least one delay adjuster coupled to the at least one phase comparator and responsive to the at least one compensation signal, for delaying at least one of the first signal and the second signal to compensate for the phase difference between the first signal and the second signal.

11. The system of claim 10 wherein the at least one delay adjuster comprises at least one adjustable delay buffer.

12. The system of claim 11 wherein the at least one phase comparator comprises:

a rising edge phase comparator for comparing a rising edge of the first signal with a rising edge of the second signal, for generating at least one rising edge compensation signal indicative of a phase difference between the rising edge of the first signal and the rising edge of the second signal; and

a falling edge phase comparator for comparing a falling edge of the first signal with a falling edge of the second signal, for generating at least one falling edge compensation signal indicative of a phase difference

between the falling edge of the first signal and the falling edge of the second signal.

13. The system of claim 12 wherein the at least one adjustable delay buffer :

delays the rising edge of at least one of the first signal and the second signal in response to the rising edge compensation signal; and

delays the falling edge of at least one of the first signal and the second signal in response to the falling edge compensation signal.

14. The system of claim 11 wherein the at least one adjustable delay buffer comprises:

at least one buffer transistor for buffering the first signal; and

at least one control transistor, responsive to the at least one compensation signal, for adjusting current flow through the at least one buffer transistor for controlling delay of the first signal through the at least one buffer transistor.

15. An integrated circuit including circuitry for compensating for phase differences between a plurality of clock signals, comprising:

a level adjuster for modifying a signal level of a signal to generate a first signal associated with a first signal level that is different than a second signal level associated with a second signal;

at least one phase comparator for comparing a phase of the first signal with a phase of the second signal, and for generating at least one compensation signal indicative of

a phase difference between the first signal and the second signal ; and

at least one delay adjuster coupled to the at least one phase comparator and responsive to the at least one compensation signal, for delaying at least one of the first signal and the second signal to compensate for the phase difference between the first signal and the second signal.

16. The integrated circuit of claim 15 wherein the integrated circuit comprises an gigabit ethernet transceiver.

17. The integrated circuit of claim 16 wherein the first signal comprises a clock signal that is associated with at least one of a near end crosstalk canceller, an echo canceller and a decision feed back equalizer.

18. A circuit for compensating for phase differences between a plurality of signals associated with a plurality of signal levels, comprising:

a rising edge phase comparator for comparing a rising edge of a first signal associated with a first signal level with a rising edge of a second signal associated with a second signal level, for generating a rising edge compensation signal indicative of a phase difference between the rising edge of the first signal and the rising edge of the second signal;

a falling edge phase comparator for comparing a falling edge of the first signal with a falling edge of the second signal, for generating a falling edge compensation signal indicative of a phase difference between the falling edge of the first signal and the falling edge of the second signal; and

an adjustable delay buffer coupled to the rising edge comparator and the falling edge comparator, for delaying the rising edge of the first signal in response to the rising edge

compensation signal and for delaying the falling edge of the first signal in response to the falling edge compensation signal.

19. The circuit of claim 18 wherein the adjustable delay buffer comprises:

at least one buffer transistor for buffering the first signal;

at least one rising edge control transistor, responsive to the rising edge compensation signal, for adjusting current flow through the at least one buffer transistor for controlling delay of the rising edge of the first signal through the at least one buffer transistor; and

at least one falling edge control transistor, responsive to the falling edge compensation signal, for adjusting current flow through the at least one buffer transistor for controlling the delay of the falling edge of the first signal through the at least one buffer transistor.

20. The circuit of claim 19 wherein:

the rising edge phase comparator comprises a register for determining whether the rising edge of the first signal leads the rising edge of the second signal; and

the falling edge phase comparator comprises a register for determining whether the falling edge of the second signal leads the falling edge of the first signal.

21. The circuit of claim 20 further comprising a plurality of low pass filters for filtering the rising edge compensation signal and the falling edge compensation signal.

22. A circuit for compensating for phase differences between a plurality of signals associated with a plurality of signal levels, comprising:

at least one phase comparator for comparing a phase of a first signal associated with a first signal level with a phase of a second signal associated with a second signal level, and for generating at least one compensation signal indicative of a phase difference between the first signal and the second signal;

a plurality of delay elements for selectively delaying the first signal; and

a delay selector coupled to the at least one comparator and responsive to the at least one compensation signal, for selectively routing the first signal through at least one of the plurality of delay elements to compensate for the phase difference between the first signal and the second signal.

23. The circuit of claim 22 wherein the at least one phase comparator comprises at least one flip-flop.

24. The circuit of claim 22 wherein the plurality of delay elements comprise a plurality of buffers.

25. The circuit of claim 22 wherein the plurality of delay elements comprise a plurality of multiplexers.

26. A method for compensating for phase differences between a plurality of signals associated with a plurality of signal levels, comprising the steps of:

generating a first signal associated with a first signal level;

generating a second signal associated with a second signal level;

comparing a phase of the first signal with a phase of the second signal to generate at least one compensation signal indicative of a phase difference between the first signal and the second signal; and

delaying the first signal to compensate for the phase difference between the first signal and the second signal.

27. The method of claim 26 wherein:

the comparing step further comprises the steps of:

comparing a rising edge of the first signal with a rising edge of the second signal to generate a rising edge compensation signal indicative of a phase difference between the rising edge of the first signal and the rising edge of the second signal; and

comparing a falling edge of the first signal with a falling edge of the second signal to generate a falling edge compensation signal indicative of a phase difference between the falling edge of the first signal and the falling edge of the second signal; and the delaying step further comprises the steps of:

delaying the rising edge of the first signal in response to the rising edge compensation signal; and

delaying the falling edge of the first signal in response to the falling edge compensation signal.

28. The method of claim 26 further comprising the step of selectively routing the first signal through at least one of a plurality of delay elements to compensate for the phase difference between the first signal and the second signal.

29. The method of claim 26 further comprising the steps of generating the first signal and the second signal with a plurality of clock trees.